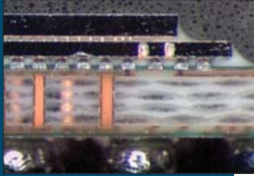
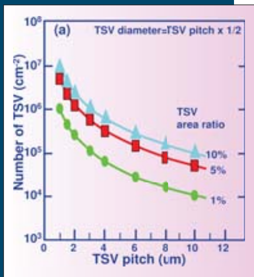
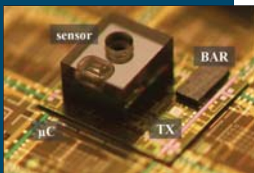
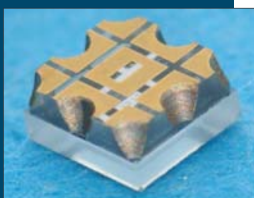
3D Through Silicon Via:
Infrastructure and Markets

Publication date: January 2010









3D Through-hole silicon via (TSV) is moving from R&D into production. Drivers for the adoption of technology included performance and form factor. Different needs and economic factors determine the timing of adoption in each application. This analysis provides an updated timeline for the adoption of the technology with realistic market projections for unit volumes and number of wafers by application.

The report also highlights the major processes and materials moving into production, including via fabrication methods, via filling, wafer thinning, and bonding methods. Assembly issues are discussed. This critical infrastructure examination provides an insight into infrastructure status and developments. The report provides an update on activities of companies and research organizations. Key barriers to 3D TSV adoption are reviewed with special emphasis on design, thermal, and test issues. Full text analysis provides critical details of the new developments and applications.

Executive Summary
- Drivers, Markets, and Infrastructure for TSV

1 Drivers for 3D Integration
- 1.1 Advantages of 3D Integration
- 1.2 Device Scaling
  - 1.2.1 Transistor Gate Delay
  - 1.2.2 Interconnect Scaling
  - 1.2.3 Resistance of Copper Interconnect
  - 1.2.4 Clock Rates
  - 1.2.5 Bandwidth
  - 1.2.6 Memory Latency
  - 1.2.7 Cost of Future Scaling
  - 1.2.8 The 3D IC Option

2 3D IC Integration
- 2.1 Reduction in Global Wiring
- 2.2 Power Consumption and Noise
- 2.3 Heterogeneous Integration
- 2.4 Circuit Partitioning, TSV Size, and Density
- 2.5 Functional Block Libraries
- 2.6 3D IC Process Sequences
- 2.7 TSV Fabrication
- 2.8 Thinning
- 2.9 Bonding
- 2.10 Wafer-to-Wafer vs.Die-to-Wafer Stacking
- 2.11 Bulk Silicon versus SOI

3 3D IC Processing
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  - 3.1.1 TSV Etch
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  - 3.1.3 TSV Isolation
  - 3.1.4 Barrier/Adhesion/Seed Layers
  - 3.1.5 Copper Plating
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  - 3.1.7 Doped Polysilicon
  - 3.1.8 Wet Via Fill
- 3.2 Wafer Thinning
  - 3.2.1 Temporary Bonding
  - 3.2.2 Influence of Thinning on CMOS Devices
- 3.3 Backside Processing
- 3.4 Permanent Bonding
  - 3.4.1 Alignment
  - 3.4.2 Bonding Options
- 3.5 TSV Reliability (Tungsten and Copper)

4 Company Activities
- AMD, ASE, ALLVIA, Amkor, Altera, DNP, Elpida, Fujitsu, Ibiden, IBM, Infineon, Intel, IPDIA, Micron, NEC, Oki Electric, Omron, Renesas, Samsung, Shinko Electric, siXis, STATS ChipPAC, STMicroelectronics, Tessera, TI, Tezzaron, Toshiba, TSMC, UMC, Xilinx, Ziptronix, ZyCube

5 Consortia and Institutes
- Albany Packaging Technology Center, ASET, CEA Leti, eCUBES, EMC-3D, DARPA, Fraunhofer-IZM, Honda Research Institute, IME, IMEC, ITRI, KAIST, Lincoln Labs, Research Triangle Institute, Sandia National Labs, SEMATECH

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6 3D IC Design Tools
- 6.1 Commercial Activities
  - Cadence, Mentor Graphics, R3Logic, Synopsys
- 6.2 University Research
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7 Thermal Management
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- Forecast for CPU Processors with TSVs
- Forecast for Graphics Processors with TSVs
- Forecast for FPGAs with TSVs
- Forecast for Wireless Applications with TSVs

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