3D IC Gap Analysis:
Remaining Issues, Solutions, Market Status

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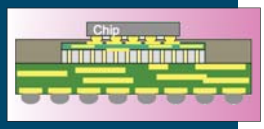

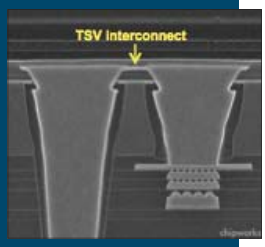

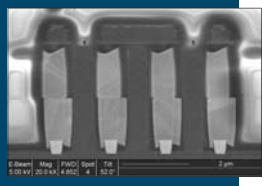

Major DRAM makers Micron, SK Hynix, and Samsung have announced versions of stacked memory with through silicon vias (TSVs) for high-performance applications. Some CMOS image sensors are also in production with die stacking and TSVs. The remaining question is what is holding back the expansion of 3D IC in other applications?

While great progress has been made in via formation and filling, process steps such as debonding during wafer thinning remain problematic. Improvements in process yield that lower cost are necessary to expand into new applications. Progress has been made in design tools and methodology, but additional work is required. Cost-effective thermal solutions are still required for memory/logic and logic/logic stacks. Progress in the testing area has been reported, but work is still needed.

This report examines challenges in adopting the technology and a timeframe for high-volume manufacturing with details of each application and its requirements. The 135-page report with full references provides market forecasts for 3D ICs in wafers and units. New developments, applications, and a market forecast for (2.5D) interposers are provided in number of wafers and units. The status of interposer suppliers, the role of OSATs, and the potential for laminate and glass interposers are discussed. A complimentary set of more than 120 PowerPoint slides accompanies the report.

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