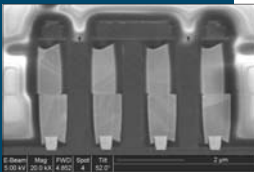
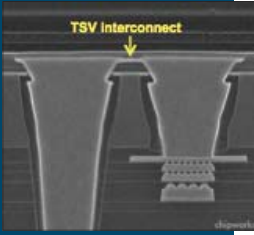
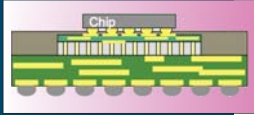


3D IC Gap Analysis: *Remaining Issues, Solutions, Market Status*

Publication date: September 2014



Major DRAM makers Micron, SK Hynix, and Samsung have announced versions of stacked memory with through silicon vias (TSVs) for high-performance applications. Some CMOS image sensors are also in production with die stacking and TSVs. The remaining question is what is holding back the expansion of 3D IC in other applications?

While great progress has been made in via formation and filling, process steps such as debonding during wafer thinning remain problematic. Improvements in process yield that lower cost are necessary to expand into new applications. Progress has been made in design tools and methodology, but additional work is required. Cost-effective thermal solutions are still required for memory/logic and logic/logic stacks. Progress in the testing area has been reported, but work is still needed.

This report examines challenges in adopting the technology and a timeframe for high-volume manufacturing with details of each application and its requirements. The 135-page report with full references provides market forecasts for 3D ICs in wafers and units. New developments, applications, and a market forecast for (2.5D) interposers are provided in number of wafers and units. The status of interposer suppliers, the role of OSATs, and the potential for laminate and glass interposers are discussed. A complimentary set of more than 120 PowerPoint slides accompanies the report.

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Amkor, ASE, PTI, Shinko Electric, SPIL, STATS ChipPAC

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ALLVIA, Dai Nippon Printing, EPWorks, GLOBALFOUNDRIES, IBM, Inotera, IMT, IPDIA, Shinko Electric, Silex, TSMC, Novati, TowerJazz, UMC

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ASET, CEA-LETI, Georgia Tech, GINTI, HDPUJ, KAIST, Fraunhofer, IME, IMEC, ITRI, NCAP, RTI, SEMATECH, STARC, Si2

- 3D IC adoption timeline.
- Trade-offs in back-side RDL for a logic-on-logic stack.
- Signal and power integrity analysis on a silicon interposer.
- Wafer chipping resulting from too soft adhesive.
- Mechanical debonding.
- Direct Bond Interconnect (DBI®) hybrid bonding.
- Bump pitch trends for TSV wafers.
- Chip on interposer on substrate.
- Thermal issue for 3D IC vs. PoP.
- Validation results of CielSpot-CTM simulation.
- EMIB conceptual drawing.
- Sony's image sensor with TSV.
- SK Hynix HBM.
- Micron's packaged die stack.
- Interposer Adoption Timeline and Barriers
- Shipments of 3D ICs with TSVs (including image sensors)
- TSV Interposer Market Projections
- 3D IC Applications: Drivers, Status, and Barriers
- Commercial EDA Tools
- Bond/Debond Equipment Offerings
- Temporary Bonding Material Options
- High Precision Bonders
- Foundry Process Offerings
- OSATs Process Offerings
- Silicon Interposer Suppliers
- Coarse Pitch and Fine Pitch Silicon Interposers
- Advantages and Challenges of Glass Interposers
- Design Rule Targets for 2.5D Glass Interposers
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- Selected Organic Interposer Suppliers and Technology
- Selected Thermally-Aware Design Solutions for 3D-TSV
- Probe Card Examples
- MCM, Interposer, and 3D IC Options
- TSV DRAM Memory Solutions
- 3D IC with TSV 300mm Wafer Shipments
- Selected Applications for Silicon Interposers
- Interposer Adoption Timeline and Barriers

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