GLOBAL SEMICONDUCTOR PACKAGING MATERIALS OUTLOOK

Produced by SEMI and TechSearch International, Inc.

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Executive Summary

SEMI® and TechSearch International, Inc. have cooperated in the development of the seventh edition of the *Global Semiconductor Packaging Materials Outlook,* a comprehensive market research study on the semiconductor packaging materials market. Interviews were conducted with more than 150 semiconductor manufacturers, packaging subcontractors, fabless semiconductor companies, and packaging material suppliers to gather information for this report. The following semiconductor packaging materials segments are covered: substrates, leadframes, bonding wire, mold compounds, underfill materials, liquid encapsulants, die attach materials, solder balls, wafer level package dielectrics, and thermal interface materials. All of the information contained in this report was developed by SEMI and/or TechSearch International.

Over the past decade, new packaging form factors have enabled the rapid growth in mobile electronics with an accompanying increase in product functionality. These form factors are smaller and thinner than packaging solutions associated with typical PC and industrial applications of the past; and such packages are becoming increasingly more complex as more functional integration is occurring for System in Package (SiP) applications. In addition to miniaturization and integration, the trend in electronics is towards lower power consumption, lower cost, and in many applications, higher reliability solutions in a smaller footprint. To achieve all of this, advancements in assembly processes and materials technologies are needed in packaging.

While innovation and new product development advances, the semiconductor industry has encountered challenges as the overall industry growth rate has slowed and development costs have risen. One consequence of lower industry growth is that companies throughout the industry value chain are consolidating, including the packaging subcontractors and as well as the material and equipment supplier bases. The overall outlook for the semiconductor industry points toward single-digit revenue and unit growth over the next several years. The semiconductor industry will continue to be driven by smartphones and other mobile products, and the emerging wearables market through 2019.

There are, however, industry segments that will experience stronger growth. Specific to packaging, advanced packaging technologies are forecasted to experience unit growth rates of 10% to 15% through 2019. Wafer-level packaging is forecasted to grow as much as 10% through the same period. The fan-out WLP (FO-WLP) approach is an example of this, as it allows device makers to maintain the same WLP size with a die shrink, increase the I/O count, and deliver heterogeneous integration/SiP in a substrate-less package thinner than a flip chip package. As a result, FO-WLP is emerging as a disruptive technology impacting shipments of laminate flip chip CSP substrates in the next three to five years. It is a disruptive because there is no substrate and thin-film metallization is used for interconnect instead of bumps or wires. Future cost and reliability targets will require new material developments for FO-WLP.

At the higher end of the packaging I/O count spectrum, flip chip applications utilizing copper pillar interconnects are growing rapidly for applications requiring high I/O and high bandwidth performance in a reduced footprint. Solutions include flip chip CSP for

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application processors and baseband devices in mobile products. Fine pitch flip chip assembly and packaging technologies will enable applications using devices fabricated with 10 nm and below process technologies.

The emerging wearables market will have diverse packaging requirements depending on the product application, the end use environment, and reliability needs. Thin and small are a must though like other applications cost versus performance will determine what package type is adopted for a given wearable product. For the most cost sensitive products, wirebonded and leadframe based packages will most likely be the preferred solution.

In discussions with material suppliers and their customers, cost issues continue to dominate the discussion as the end electronics market demands low cost solutions for the consumer. Packaging material customers specifically highlighted concerns with supply chain stability in some segments such as leadframes. In this market segment, there has been some consolidation and restructuring of the supplier base, including that of the base alloy suppliers. In addition, China suppliers are emerging, especially for liquid encapsulants for LED, copper and silver bonding wire, and leadframes (and though currently not covered in this report, plating chemicals for packaging applications).

Advancements and changes continue in the semiconductor packaging materials market, and over the next several years some areas of opportunity include:

- Continuing cost reductions across all material and process sets
- Targeting <5 µm lines and spaces and 40 µm via diameters in the build-up layers for substrates. Roadmaps show core layers with 20 µm lines and spaces with vias as small as 50 µm and capture pads as small as 110 µm
- New film materials with improved surface roughness to support finer line and spaces and new build-up films with smoother surfaces to enable finer traces with stronger adhesion
- Low CTE materials for the substrate core are desired to limit warpage.
- Adoption and ramp of coreless structures based on a modified leadframe technology called a Molded Interconnect Solution/System (MIS). Advancements are needed to further the high-volume ramp of MIS and other routable-QFN technologies
- Expansion of photoresist plating capability for selective plating of leadframes
- For copper wire, softer and more reliable materials to further improve mechanical properties and enable advancements in wire bonding
- Copper and silver wire for low looping and multi-die applications
- Advanced mold compounds for array, small form factor, and 3-D packages that address warpage and reliability issues
- Mold compounds to provide underfill for copper pillar flip chip
- Thermally enhanced and high-voltage mold compounds for power and automotive devices
- New underfill resin and filler formulations to address the smaller gaps and fine pitch flip chip and with some stacked-die applications
- Reworkable underfill for packaging applications
- Improve stability and refractive index of LED encapsulants
- Both die attach pastes and films need to satisfy tighter control of bondline thickness and fillet formation, including conductive die attach films (CDAF) materials
- Thermally conductive die attach materials other than solder die attach are needed for power applications including nano-particle sintered and Transient Liquid Phase Sintering (TLPS) die attach materials.
- Certified conflict free metals for solder balls

- WLP dielectrics to support fine features roadmaps (≤5 µm lines and spaces) and split die or multi-die packaging/ system-in-package (SiP)
- WLP dielectrics with good adhesion to metal (Cu) layers and epoxy (in the case of FO-WLP reconstituted wafer) without delamination
- Low stress WLP dielectric (to match the CTE of the chip) and/or low modulus (for less wafer bow)
- WLP materials technology and processes for future panel production
- TIM development to improve wetting and coupling of the resin to the filler, and the increasing thermal transfer between the two for thinner bondlines
- New fillers and formulations for TIM applications, including nano-fibers, nanowire, and graphene

In total, the semiconductor packaging materials market covered in this study was $17.7 billion in 2014 globally, and it is forecasted to be $17.4 billion in 2019, excluding thermal interface materials. The market size including thermal interface materials was $18.5 billion in 2014. The constrained revenue growth is due to cost reduction pressures and the trend towards lower material consumption with the growth in smaller and thinner packaging form factors. Material units are expected to undergo steady single-digit unit volume growth for many material segments through 2019, including laminate substrates, IC leadframes, underfill, and copper wire. Segments such as wafer-level packaging (WLP) dielectrics will experience stronger unit volume growth over the same timeframe.

The global market for laminate substrates for IC packages is forecasted to experience a compound annual growth rate (CAGR) of 3% from 2014 through 2019 on the basis of square meters of materials processed. The growth rate for flip chip PGA/LGA laminates remains the highest of the segments, while wire bond PBGA substrates will decline over the forecast period. The substrates of the future may also require new process capabilities with changes in processing chemicals expected to be required and a possible move to processes more commonly found in IC fabrication such as steppers for lithography tools, new methods of material deposition, and planarization using CMP tools.

Overall leadframe shipments are forecasted to grow at a 3.2% CAGR from 2014 through to 2019, with LFCSP (QFN type) experiencing the strongest unit growth. Over the same period, leadframe revenues are forecasted to decline by -1.2% CAGR.

Gold wire represented 44% of the total bonding wire shipments in 2014, with total copper wire at about 48% share of the shipments. Total wire shipments will reach just under 20 billion meters shipped in 2015, with total shipments forecasted to grow under 2% CAGR through to 2019. Copper bonding wire will have a 55% share of the shipments and silver will grow to a 13% share by 2019.

For mold compound revenues, the 2014 to 2019 CAGR will be just 0.2%. Revenues declined to $1.2 billion in 2015, due to, in large part, the weaker Yen. Japanese headquarter suppliers are estimated to have over a 70% share of this market.

The main application for underfill remains flip chip packaging, but as bump pitches shrink limitations of the current capillary UF process and materials demand that alternatives be explored. Molded underfill (MUF) is one approach. Much of today's underfill development work is focused on non-conductive film (NCF) as the thin, uniform film layer has advantages over the other avenues. The tight control makes NCF an ideal component for thin-die applications. The total underfill market was $241 million in 2014 and will grow at a CAGR of about 3% through 2019. Volume growth will be above 5% CAGR.

Liquid encapsulant revenues were $1.0 billion in 2014 and the CAGR through 2019 is expected to approach 8%. LED packaging applications are driving the revenue growth over the forecast period. China-based suppliers are expected to gain share in the China market.

Die attach material revenues will reach $664 million in 2014 and with an estimated CAGR of 3.2% through to 2019. DAF materials will undergo higher unit growth. Reliability with respect to die attach bondline and fillet control are becoming increasingly more critical in thin/small die applications.

Solder ball revenues will be $151 million in 2014 and will grow by 6% CAGR through to 2019. The revenues are much lower compared to figures presented in the previous report as lower metal prices and the entrance of new suppliers from China have spurred dramatic declines in pricing. A number of companies have exited the solder ball business in the last several years.

The WLP dielectrics market is forecasted to grow from $81 million by over 10% CAGR to 2019. Fan-out WLPs (FO-WLPs) are an increasingly popular alternative to the conventional fan-in WLPs so development is centered on materials and processes to support increased I/O density. Another goal in WLPs is to reduce the number of mask steps, which would simplify the process in order to reduce costs.

Thermal interface material (TIM) is needed to manage thermal performance as power density increases in many device applications. New materials and approaches are being developed so to advance TIM performance. These include development of polymer and fillers for higher-performance thermal greases, lightly-crosslinked gels, and phase-change materials. The TIM market was $775 million in 2014 and will grow at a 5.6% CAGR to 2019.

Estimated 2015 global market size and key trends in each semiconductor packaging materials segment are summarized in the following Table (page 4).

ESTIMATED 2015 GLOBAL MARKET SIZE AND KEY TRENDS IN SEMICONDUCTOR PACKAGING MATERIALS SEGMENTS

Semiconductor Packaging Materials Segment	Estimated 2015 Global Market Size $M	Comments
Laminate Substrates	$7,779	New substrates introduced with the objective of achieving high density, but at a lower cost than silicon interposers. Pressure from low-end MIS packages and the high-density FO-WLPs may result in lower prices in the future. Some suppliers are expected to focus on emerging package formats such as SiP.
Leadframes	$2,991	LFCSP is the strongest unit growth driver. Interest in routable, high-density QFN is increasing. Manufacturing investments are focused on etched leadframes and plating/surface treatments.
Bonding Wire	$2,924	Gold has declined to 42% share of shipments. New entrants have increase position in the market for copper and silver wire.
Mold Compounds	$1,208	Declining/low volume growth with industry trend towards smaller/ thinner package form factors. Warpage control continues to drive materials development. Growth in compression molding processes.
Underfill Materials	$255	CUF technology is being pushed as package geometries shrink. Companies are considering the use of vacuum-assist to improve the flow of the underfill material. Package underfill to pass drop test in mobile products
Liquid Encapsulants	$1,120	Strong market growth in LED applications though declining ASPs. The emerging supplier base in China for the LED market is expanding its material offerings.
Die Attach Materials	$679	Bondline control and fillet formation are critical to yield and reliability in a small, thin form factor. Strong interest in CDAF and other thermally enhanced die attach material solutions.
Solder Balls	$169	Lead-free balls represent 99% of shipments. Price declines with lower base metal prices. Some suppliers certify the use of conflict-free metals. Several suppliers have exited the market.
Wafer Level Package Dielectrics	$89	Fan-out WLPs (FO-WLPs) are an increasingly popular alternative to conventional fan-in WLPs. Emerging split die or multi-die packaging/ system-in-package applications.
Thermal Interface Materials	$817	Lower cost material, higher yield, part count reduction and easier handling for automation. Fragmented TIM2 market with a large number of players.

Source: SEMI Industry Research and Statistics and TechSearch International, December 2015