PRESS RELEASE

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TechSearch International Quantifies Heterogeneous Integration Market Growth Including Chiplets and SiP

The market for heterogeneous integration is projected to grow 10% in number of packages from 2020 to 2025, reaching almost 54 billion packages. Smartphones, wearables, and consumer packages account for the largest number. RF front-end modules including the latest 5G mmWave modules and wireless connectivity modules for Wi-Fi, Bluetooth, and other networks account for nearly half of all heterogeneous integration devices counted in this report. High-performance computing, 5G telecommunications infrastructure, networking, stacked memory, automotive, and medical applications also contribute to the growth in heterogeneous integration packages.

The market for packages using chiplets is expected to show a CAGR of 104% from 2020 to 2025. A chiplet is a functional circuit block and includes reusable IP blocks. It is a physically realized and tested IP with a standard or proprietary communication interface between IP blocks. A chiplet functions with other chiplets, so the design must be co-optimized and the silicon cannot be designed in isolation. An increasing number of companies are turning to chiplets to achieve the economic advantages lost with expensive monolithic scaling, ushering in a new era of smart packaging. The adoption of chiplets represents an inflection point in IC design for CPUs and GPUs; similar to the transition from perimeter pad design to area array with the adoption of flip chip interconnect. It is also possible to have higher core counts and therefore higher performance than with a monolithic design. There is a potential for improved power distribution. Binning the chiplets provides an opportunity to optimize performance even further. Chiplets have been adopted for server processors and AI accelerators, desktop and laptop processors, networking, and adoption in mobile applications such as smartphones and tablets is anticipated. Chiplets can be configured side-by-side or as a 3D stack. The 3D stack may use microbumps, but the direct Cu-to-Cu bonding method provides some of the greatest density and electrical advantages.

Quantifying the Impact of Heterogeneous Integration: Chiplets and SiP is a 130-page report with full references and an accompanying set of 122 PowerPoint slides.

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